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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,110	08/01/2003	John Pasternak	SAND-01013US0	3624

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,110	PASTERNAK, JOHN	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 is indefinite because it is unclear that the "voltage detector" recited in claim 2 is the same as the voltage detector recited in claim 1.

Claims objection

Claim 27 is objected because the limitation "a threshold" in line 3 has been recited in line 2.

Claim 33 is objected because it recites the same limitations as claim 20.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 5-17, 19, 20 and 25-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Morishita (USP 6329873).

As to claim 1, Morishita discloses in figure 8 a memory system including a control path to a host device (circuits 2 and 3 in figure 1) supplying a voltage, comprising a voltage regulator (DRm) including an input (source), an output (drain) and a bypass (1h) shorting the input to the output, a voltage detector (the comparator in MA) communicating with the regulator; a bypass enable signal (ZSIG) operable responsive to a signal (ACT) generated by the host device indicating that the power up of the host is complete *(the external supply voltage must be high enough (power up) in order for circuit 2 in figure 1 to generate signal ACT).*

As to claim 2, figure 8 shows a voltage detector (1a) outputting a signal (SIG) indicative of the host supply voltage.

As to claim 3, figure 8 shows that the bypass is at least one transistor.

As to claim 5, figure 8 shows that the bypass enable signal provided by the controller (circuit 2 in figure 1) to a gate of the transistor.

As to claim 6, figure 8 shows that the signal generated by the host device is a command signal to the memory system.

As to claims 7, 11-15, it is seen as in intended use for using the voltage regulator in figure 8 in a multimedia card, PC card, compact flash card, secure digital card, media smart card, or memory stick.

As to claim 8, figure 8 shows that the the signal generated by the host device is a command signal, and it is it is seen as in intended use for using the voltage regulator in figure 8 in a multimedia card.

As to claim 9, figure 8 shows that the command CMD0 signal or CMD1signal.

As to claim 10, it is inherent that the signal (ACT) generated by the host is a signal indicating power up of the host device is complete (see the rejection of claim 1).

As to claim 16, figure 8 shows a method for operating a voltage regulator in a memory system, comprising: providing a voltage regulator (SA and DRm) having an input and an output, and including a regulator bypass (1h) shorting the input to the output; setting the bypass to off prior to power up of a host device (*circuits 2 and 3 in figure 1. It is noted that signal Act is generated after the external power supply voltage is up, see the rejection of claim 1*), responsive to a power up completion signal (ACT) from a host device, determining the power supplied by the host; and if the power is below a threshold operating voltage (Vref), enabling the bypass.

As to claim 17, figure 8 shows that the bypass is a transistor and the step of setting the bypass to off includes providing a signal to a gate of the transistor.

As to claim 19, figure 8 shows that the power up completion signal is a command signal from the host.

As to claim 20, figure 8 shows that command signal is CMD0 or CMD1 for a multimedia card. It is see as an intended use for using the voltage regulator figure 8 in a multimedia card.

As to claim 25, figure 8 shows a peripheral device for a host system (figure 1) including a voltage regulator circuit, comprising: a voltage regulator (SA and DRm) having an input and an output; a bypass element (1h) coupled to selectively short the input to the output, a bypass control signal (ZSIG) coupled to the bypass element and responsive to a host system power up completed signal (ACT) which enables the bypass element when the voltage provided by the host is below a threshold level.

As to claim 26, figure 8 shows the regulator includes a detector (1a, see further figure 10)) responsive to the power up completed signal.

As to claim 27, figure 8 shows the detector outputs a first signal (low) when the voltage provided by the host is above a threshold (Vref) and a second signal (high) when the host is below a threshold.

As to claim 28, figure 8 shows that the bypass element includes at least one p-type transistor.

As to claim 29, figure 8 shows that the bypass control signal is applied to the gate of the at least one transistor.

As to claim 30, figure 8 shows that the bypass element is disabled during power up of the host device (the ACT signal will not generated after circuit 2 in figure 1 receive enough power).

As to claim 31, figure 8 shows that the bypass control signal is provided by a controller.

Claims 32-36 recite similar limitations with at least one of the claims above. Therefore, they are rejected for the same reasons. As further called in for claim 34, it is inherent that Morishita's memory circuit having memory array.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morishita (USP 6329873) in view of Hellums (USP 5362988).

Morishita's figure 8 shows all limitations of the claim except for transistor 1h comprises plurality of transistors. However, Hellums teaches in figure 1 that transistor 28 is made of plurality of transistors for the purpose of increasing the pull up speed. Therefore, it would have been obvious to one having ordinary skill in the art to make Morishita's transistor 1h with plurality of parallel connected transistors for the purpose of increasing the pull up speed.

7. Claims 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morishita (USP 6329873).

Morishita's figure 8 shows all limitations of the claims except for the threshold voltage is below 2.7v, 2.0v, 1.65v or 1.3 volt. However, the selection of the threshold voltage to be below 2.7v, 2.0v, 1.65v or 1.3 volt is seen as an obvious design preference dependent upon paricular environment of use to ensure optimum performance. Furthermore, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quan Tra
Patent Examiner

September 21, 2004